Remarks

Claims 1 – 8 and 10 are pending in this action. Claims 11 – 22 stand withdrawn and Claims 1 – 8 and 10 stand rejected. By this amendment claims 1-36 have been cancelled and claims 37-51 have been added. Applicants respectfully request reconsideration of all pending claims herein.

Applicants respectfully submit that new claims 37-51 more clearly define and claim Applicants' invention and that the drawings and specification provide sufficient enablement to meet 35 U.S.C. § 112 paragraphs 1 and 2 requirements and overcome 35 U.S.C. § 102(b) and (e) rejections.

No new matter has been added to the application by virtue of the present amendment. Support for the amendments is found in Applicants' figures 1-8 and the specification.

In the Specification

Applicants have amended paragraphs: 31, 38, 46, 79, and 95 to comply with requests for correction outlined in the Office Action pages 4-5. Applicants further submit that a single bracket ("[ ]") indicates wording that is not represented in a quotation, but exists in the actual documentation from which the quote is taken. Double brackets ("[[ ]]"), however, is the proper representation for a deletion edit. Therefore, Applicants contend that the amendments to the specification in the 7/6/06 response are correctly presented.

Regarding the conflict between the terms "circuit module" and "code module" beginning in p80, applicants amended Figure 7 to replace "circuit module 25" with "code module 25" in the RCE and amendment filed 7/6/2006. The drawings were subsequently accepted by Examiner.

Claim Rejections – 35 U.S.C. §112, first paragraph

The Office Action states that claims 1 – 8, and 10 are rejected under 35 U.S.C. §112, first paragraph, as failing to comply with the written description requirement. The Office Action stated that "claims 1 and 8 refer to a "black box circuit" which is not described in the application as filed." The Office Action further stated that "Paragraph 22 of the specification describes an "encapsulated (behaviorally equivalent) circuit". The specification contains no reference to a "black box circuit". Whether these terms are completely synonymous is unclear, however employing claim language that finds antecedent basis in the application as filed would circumvent that ambiguity."

Applicants have cancelled claims 1 and 8, and added new claims 37 and 45 to replace the references to a "black box circuit" with language from paragraph 22 of Applicants specification per Examiner's suggestion (10/16/06 Office Action pg. 7). Specifically, Applicants have added new claims 37 and 45 to recite in part: "…an encapsulated circuit model stored in the memory, the circuit model being behaviorally equivalent to an original circuit…".

Applicants respectfully submit that the language "encapsulated circuit model" is both explicitly and inherently shown/described in Applicants' specification (see para 11, 57, 80, and 89, and Fig. 1), because the wording "the internals of the specific circuit are hidden from the user" is inherently an "encapsulated circuit model". Applicants contend that "a behaviorally equivalent circuit model … which will rapidly and faithfully reproduce the original circuit's behavior during circuit simulation […] [and] simultaneously addresses […] encapsulation/topology hiding (detail hiding)" is synonymous with "encapsulated circuit model" (see Lehner para 11). Furthermore, the specification explicitly recites an "… encapsulated (behaviorally equivalent) circuit model … [which] exhibits none of the internal circuit details from the original circuit." (see Lehner para 22).

The encapsulated circuit model is clearly shown in Applicant's figures 1-5 and claimed in new claims 37-51. In Intex Rec. Corp. v. Metalast, S.A., 2005 U.S. Dist. LEXIS 10147 (D.D.C. 2005), the court stated:

> It is well-recognized that "drawings alone may provide a written description of an invention as required by § 112," (Vas-Cath, 935 F.2d at 1565); see also Koito Mfg., 381 F.3d at 1154 (stating that "the written description requirement can be satisfied by words, structures, *figures, diagrams*, formulas, etc." and relying on an illustrative figure in determining that the requirement was satisfied) (emphasis in original).

The circuit models shown in Applicants' Figures 1-5 enable one of ordinary skill in the art to create and use the model of the present invention for original circuits. The circuit models shown in Figures 1-5 incorporate the functionality of capacitors, current, and voltage sources, and are used to model an original circuit. The algorithms and method steps for creating and using an encapsulated model is shown in Applicants' Figures 6-8. The encapsulated circuit model is a representation of a proprietary or otherwise confidential circuit (i.e. intellectual property), which is provided to a customer who endeavors to use the circuit either alone or in a larger IC design.

Applicants have cancelled claims 1 and 8, and cited specific references to descriptions in Applicants' specification to overcome any new rejection to new claims 37 and 45 for failing to comply with the written description requirement. Applicants therefore submit that the 35 U.S.C. §112 first paragraph rejection of claims 1 and 8 has been overcome. The rejection of claims 2-7, and 10 has been likewise been overcome by virtue of their cancellation.

Claim Rejections – 35 U.S.C. §112, second paragraph

The Office Action stated that claims 1-8 and 10 stand rejected under 35 U.S.C. §112, second paragraph as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The Office Action stated that "the disconnect between the claim terminology and the specification, as well as the several indefinite claims, make it difficult to determine which of the recited limitations are indefinite and which are clear in light of the specification".

Specifically, claim 1 stands rejected because it "recites 'a memory for access by a circuit simulation program' and recites several subsequent limitations. The claim recites no limitations that further define 'a memory'" and that "none of the claimed limitations are clearly drawn to structural features of said memory". The Office Action further stated that, "Limitations such as 'a first and second current function' encompass an enormous breadth and fail to distinguish the invention from the prior art. In the absence of any positively recited claim limitations defining these functions, any integrated circuit device or any circuit model will have some first and second current function, although those functions may amount to no current at all. Similar analysis applies to limitations such as 'a first voltage function,' 'a first, second, and third capacitance function,' 'an internal impedance function,' etc."

Applicants have cancelled claims 1 and 8 and added new independent claims 37 and 45 to distinctly claim the circuit model as the model exists in a memory device. Claim 1 now recites:
"A memory *(e.g. Fig. 8 RAM 265, ROM 270, etc.)* for access by a circuit simulation program *(Simulator Fig. 6)* comprising: an encapsulated circuit model *(CKT A, B, C, Fig. 1, and Fig. 2)* stored in the memory, the circuit model being behaviorally equivalent to an original circuit *(p8, 11, 22, 25, 38, and 57)* the circuit model comprising at least one output node *(Fig. 2 Vout)* and one input node *(Fig. 2 Vin)*;
a first current source *(Fig. 2, Ip)* having a first current value and being connected to a voltage source and the output node;
and second current source *(Fig. 2, In)* having a second current value and being connected to the output node and ground;

a first input voltage value *(p38)*;

a first output voltage value *(p38)*;

a first capacitor *(Fig. 2 Cin)* connected to the input node and ground and having a first capacitance value;
a second capacitor *(Fig. 2 Cm)* connected to the input node and output node and having a second capacitance value; and
a third capacitor *(Fig. 2 Cout)* connected to the output node and ground and having a third

capacitance value;

wherein the circuit simulation program *(Fig. 6 "Simulator")* configures a computer system *(Fig. 8 250)* to calculate an output node value *(Fig. 6 box 61 output voltage waveforms)* on the output node of the encapsulated circuit model;

the output node value is a function of *(Fig. 6 Final Element Values)* the first and second current value *(Ip, In)*, the first input voltage value *(VI1)*, the first output voltage value *(V01)*, and the first, second and third capacitance value *(Cin, Cm , Cout)*;

wherein the first and second current value, and the first, second, and third capacitance value, is calculated by the computer system as a function of the first input voltage value and the first output voltage value *(Fig. 6, V01, VI1)*.

the computer system further stores in the memory *(Fig. 6 box 63)*, the input voltage value, the output voltage value, the first and second current value, the first, second, and third capacitance value, and the output node value;

the circuit simulation program accesses the memory to retrieve the output node value *(Fig. 6 box 61 Output Voltage Waveforms)*; and

the encapsulated circuit model stored in the memory exhibits none of a plurality of circuit details from the original circuit *(Fig. 1 and 2)*."

Thus the memory comprises the circuit model, which further comprises values stored in memory for the current values and the capacitance values, each value calculated using an input and output voltage value over a range of input and output voltage values (See Lehner Figures 1-6 and 8, para 33, 35 and equation 1). The values are retrieved from memory during circuit simulation depending on the surrounding circuits' parameters, and modified according to external environmental parameters, also supplied by the circuit simulator.

The Office Action stated that the rejection and analysis applied to claim 1 also applies to claim 8 and that "[T]he Examiner is aware of no such object as "an impedance" which can be "connected to the output node and ground." To the best of the Examiner's knowledge, impedance is a property, not an object or element with connections".

Applicants have added claim 45 to replace claim 8. Claim 45 removes any reference to an impedance. However, claims 43 and 50 have been added as dependent claims and recite in part "… an impedance *value* measured between the output node and ground." to clarify that impedance value between an output node and ground is required in some cases to simulate the encapsulated circuit model (see Lehner p24 and 46, fig. 2 and 5). Claims 44 and 51 further depend from claims 43 and 50 respectively and limit the impedance value to that derived from a pi model (Fig. 6 box 69).

Claim Rejections – 35 U.S.C. §102(b)

The Office Action stated that claims 1-3, 5-6, 8, and 10 are rejected under 35 U.S.C. 102(b) as being anticipated by "IsSpice4 User's Guide" by Intusoft. Specifically the Office Actions stated that Intusoft discloses a computer simulator software, and implicitly "a memory for access by a circuit simulation program" and that the computer memory comprises a circuit model. The Office Action further stated that Intusoft discloses that the computer memory comprises the various functions.

Applicants have cancelled claims 1-3, 5-6, 8, and 10, which overcomes the above rejection. However, in the interest of furthering prosecution, Applicants submit that "iSsPICE4 User's Guide" by Intusoft does not anticipate Applicants' now claimed invention. Most notably, IsSpice4 is a circuit simulator which can be *used* to perform an overall circuit simulation on a design which includes Applicants' claimed encapsulated circuit model (See Intusoft pg. 13 last paragraph, and Lehner p37 and 38). Additionally, IsSpice4 could be *used* by the proprietary circuit designer to

calculate the parameter values (Ip, In, Cm, Cin, Cout) stored in memory (Lehner Fig. 6 box 63) using the method steps described in Applicants' specification paragraphs 37-43. The collective parameters stored in memory make up the encapsulated circuit model and this is what is given to the customer. A Spice simulator is simply a tool for practicing Applicants' invention, including building and/or simulating the novel circuit model (Lehner Fig. 2-5). In fact, IsSpice4 is a simulator which can be used as the "circuit simulator program" defined in Applicants' claims 37 and 45. However, Intusoft's IsSpice4 simulator is not "…an encapsulated circuit model stored in the memory which is behaviorally equivalent to an original circuit… the encapsulated circuit model stored in the memory exhibits none of a plurality of circuit details from the original circuit."

Therefore, Applicants' submit that the Intusoft reference does not anticipate Applicants' now claimed invention and the U.S.C. §102(b) rejection has been overcome.

Claim Rejections – 35 U.S.C. §102(e)

The Office Action stated that claims 1-3, 5-6, 8, and 10 are rejected under 35 U.S.C. §102(e) as being anticipated by USPN 6,718,522 issued to McBride et al (McBride). The Office Action stated that McBride discloses a "black box model" and that Figure 3 reference 43 and associated description anticipate claims 1-3, 5-6, 8, and 10.

Applicants have cancelled claims 1-3, 5-6, 8, and 10, which overcomes the above rejection. However, in the interest of furthering prosecution of new claims 37-51, Applicants submit that McBride does not anticipate Applicants' invention as claimed. Specifically, McBride discloses a design rule checker system having specific design rule checking algorithms (e.g. static timing analysis, netlist for reported paths, error/slack reports, netlist files, parasitic files, etc.) stored in memory. As discussed above, it is conceivable that one could use McBride's invention to perform design rule checking on an IC design which includes Applicants' encapsulated circuit model. However, McBride does not disclose "… an encapsulated circuit model stored in the memory, the circuit model being behaviorally equivalent to an original circuit … the circuit model

comprising: … a first current source … connected to a voltage source and the output node … and second current source … connected to the output node and ground … a first input voltage value; a first output voltage value; a first capacitor connected to the input node and ground … a second capacitor connected to the input node and output node … and a third capacitor connected to the output node and ground …the encapsulated circuit model stored in the memory exhibits none of a plurality of circuit details from the original circuit."

Based on the foregoing, Applicants submit that McBride does not anticipate Applicants' claimed invention and is therefore not a 35 U.S.C. § 102(e) prior art reference. Hence the rejection under 35 U.S.C. § 102(e) is overcome.

Summary and Conclusion

Based on the foregoing, it is respectfully submitted that the pending claims in the subject patent application are in condition for allowance and that the application may be passed to issuance.

The Examiner is urged to call the undersigned at the number listed below if, in the Examiner's opinion, such a phone conference would aid in furthering the prosecution of this application.

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